

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A direct memory access controller coupled with an arbiter, which arbitrates a bus right between the direct memory access controller and another circuit, comprising:

a plurality of direct memory access transfer portions controlling direct memory access transfer ~~in accordance with values set in a group of registers for current transfer;~~

a control portion permitting use of a bus by said plurality of direct memory access transfer portions, in response to transfer requests from said plurality of direct memory access transfer portions, while the bus ownership is granted to the direct memory access controller from a bus master said arbiter; and

~~a group~~ two groups of registers including a first group for current transfer and a second group for next transfer which is different from said first group of registers for current transfer, values set in two groups being for controlling the direct memory access transfer,

wherein said control portion permits transferring to a first portion of said direct memory access transfer portions transfer based on values set in said first group of registers for next transfer to said group of registers for current transfer to control direct memory access transfer, and permits transferring to a second portion of said direct memory access transfer portions based on values set in said second group after transferring by said first portion, in one granting period of transferring by the arbiter.

~~said direct memory access controller further comprises a cycle steal control circuit receiving a control signal from an arbiter to control the control portion such that bus ownership is passed to another channel in a prescribed order and the bus ownership is passed among channels at every prescribed number of transfers.~~

2. (Cancelled)

3. (Currently Amended) The direct memory access controller according to claim 1, wherein

to said second group of registers for next transfer, direct memory access control information stored in an external memory is successively transferred and stored.

4. (Currently Amended) The direct memory access controller according to claim 3, wherein

transfer of the direct memory access control information from said external memory to said second group of registers for next transfer is performed after previous values stored in said second group of registers for next transfer to said first group for current transfer are transferred to ~~any of said plurality of direct memory access transfer portions~~ and before bus ownership is switched among said plurality of direct memory access transfer portions.

5. (Original) The direct memory access controller according to claim 1, wherein
said control portion determines order of bus use by said plurality of direct memory access transfer portions in accordance with round robin method.

6. (Original) The direct memory access controller according to claim 1, wherein said control portion determines order of bus use by said plurality of direct memory access transfer portions in accordance with past number of direct memory access transfers by each channel.

7. (Original) The direct memory access controller according to claim 1, wherein in said control portion, number of transfers made by each channel while one continuous bus ownership is being granted is set, and said control portion permits use of the bus among said plurality of direct memory access transfer portions in accordance with said number of transfers.

8. (Original) The direct memory access controller according to claim 1, wherein in said control portion, an order of bus use by channels is set when there are three or more channels, and bus use is permitted among said plurality of direct memory access transfer portions in accordance with the order of bus use.

9. (New) The direct memory access controller according to claim 1, further comprising a cycle steal control circuit,
wherein said control portion permits said first and second portions of said direct memory access transfer portions by a cycle steal manner controlled by said cycle steal control circuit.